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Fujii

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(54) **SEMICONDUCTOR DEVICE**

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(30) **Foreign Application Priority Data**

Mar. 25, 2011 (JP) 2011-068214

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H01L 23/52 (2006.01)
H01L 23/29 (2006.01)
H01L 23/31 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 23/291*** (2013.01); ***H01L 23/3157*** (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**
CPC H01L 2924/00; H01L 2224/48227; H01L 21/0254; H01L 23/291; H01L 23/3157; H01L 2924/0002
USPC 257/503, 636, 646, 490, 494, 640, 774, 257/E23.01, E21.591, E23.144, E21.627, 257/E21.641, E21.151, E29.015
See application file for complete search history.

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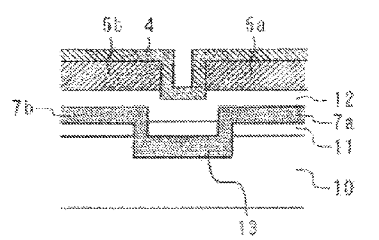
(57) **ABSTRACT**

A semiconductor device includes: a substrate; a lower wiring on the substrate; an inter-layer insulating film covering the lower wiring; first and second upper wirings on the inter-layer insulating film and separated from each other; and a semi-insulating protective film covering the first and second upper wirings, wherein the protective film is not provided in a region right above the lower wiring and between the first upper wiring and the second upper wiring.

5 Claims, 6 Drawing Sheets



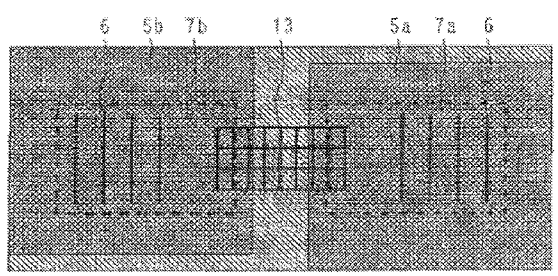


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FIG. 1

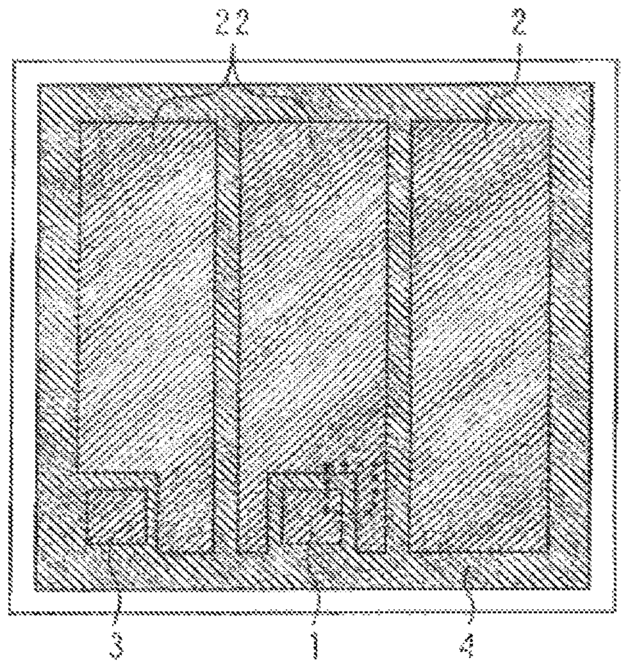


FIG. 2

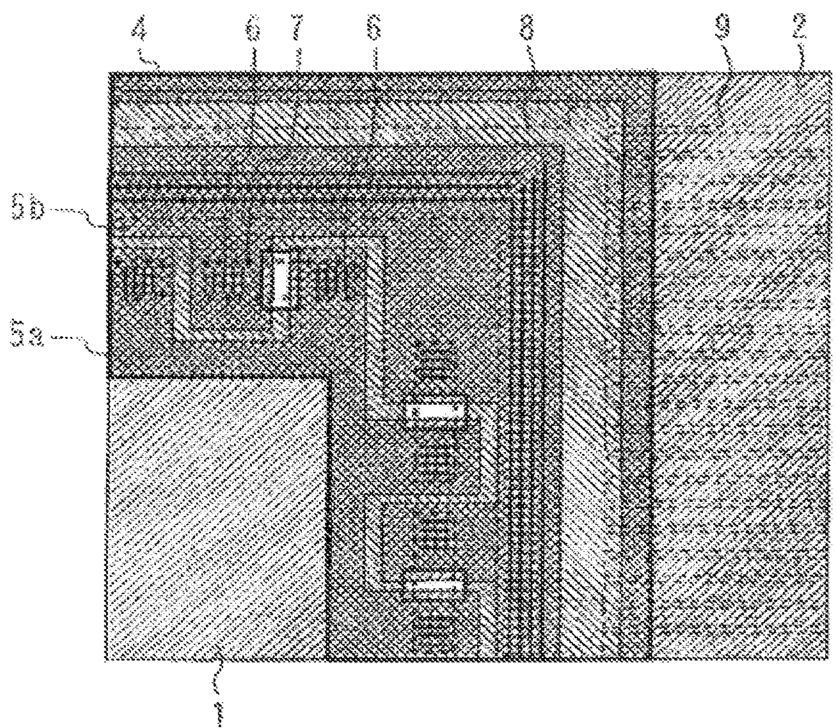


FIG. 3

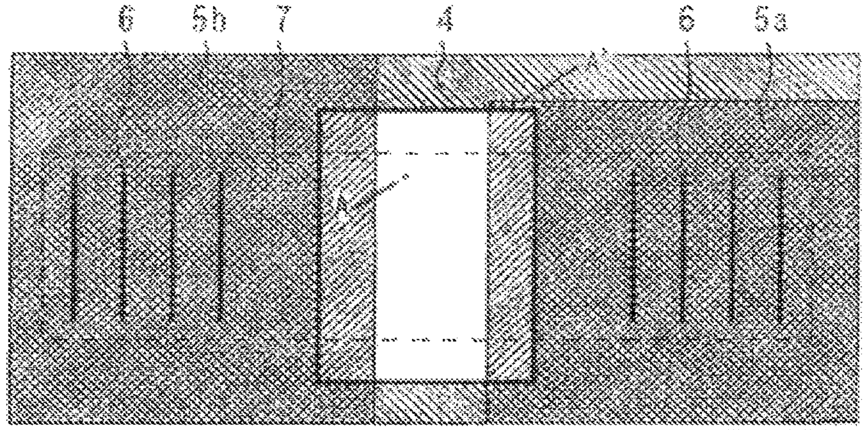


FIG. 4

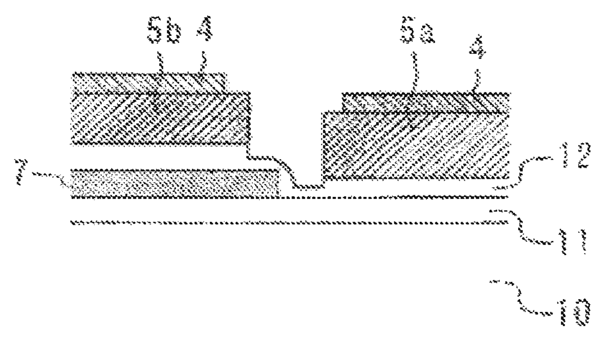


FIG. 5

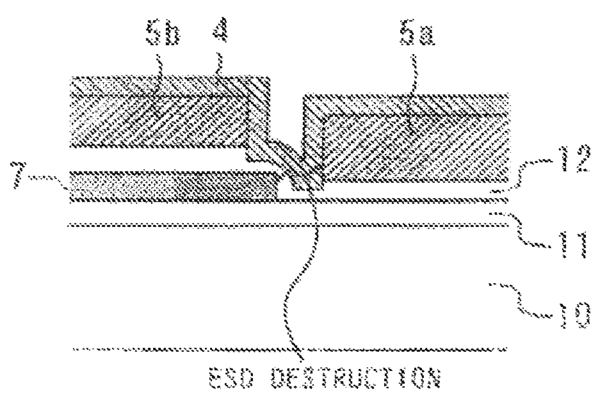


FIG. 6

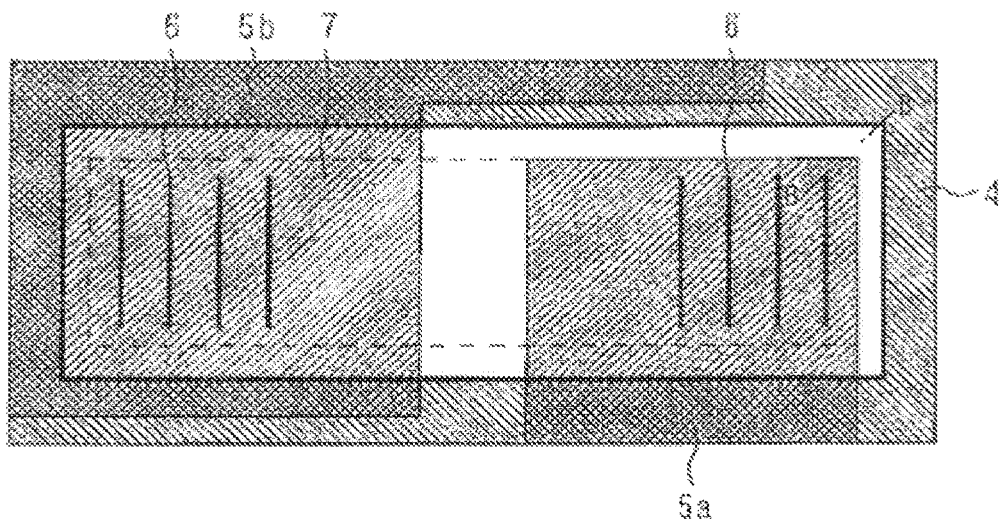


FIG. 7

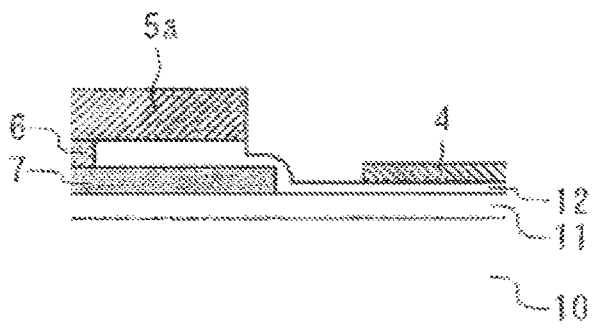


FIG. 8

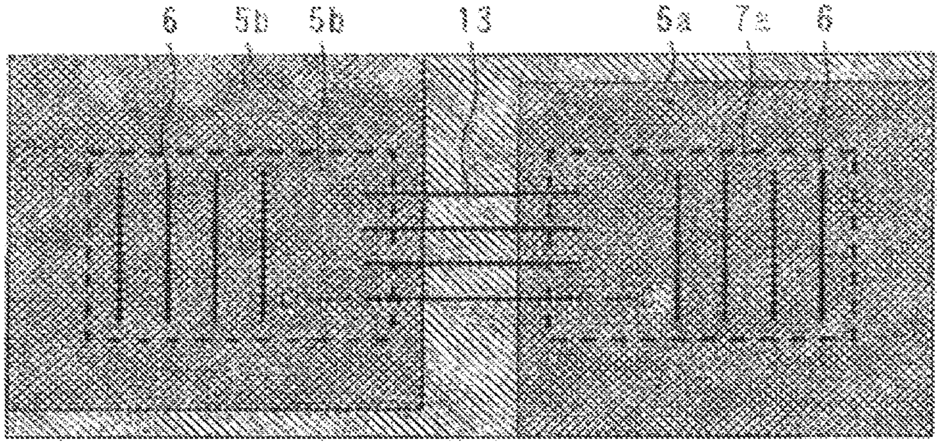


FIG. 9

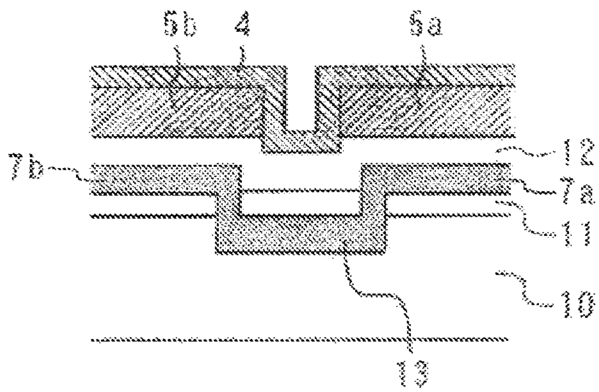


FIG. 10

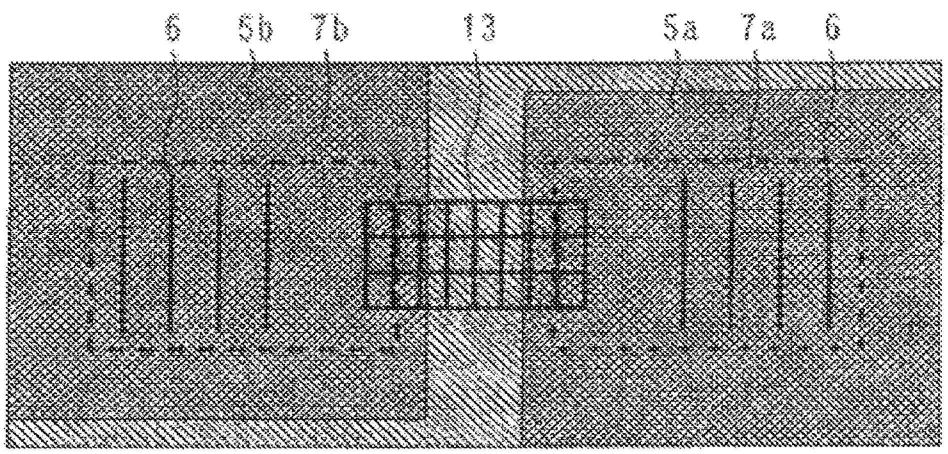


FIG. 11

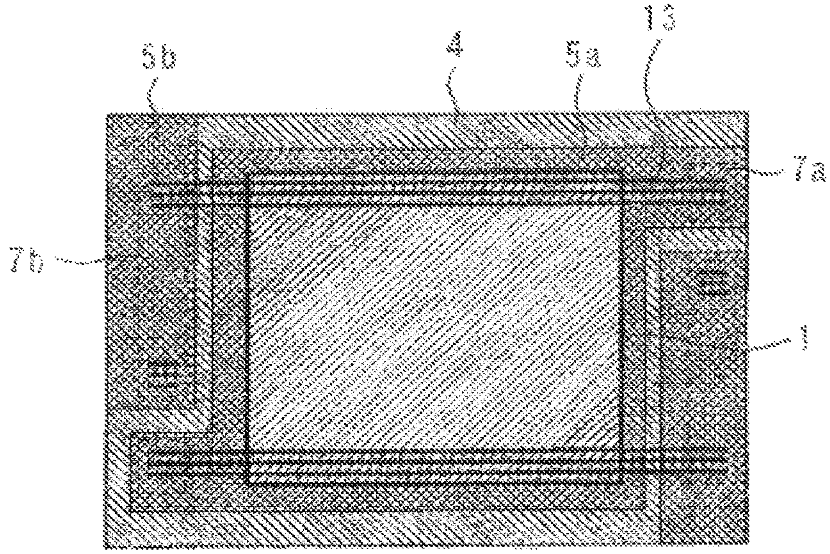


FIG. 12

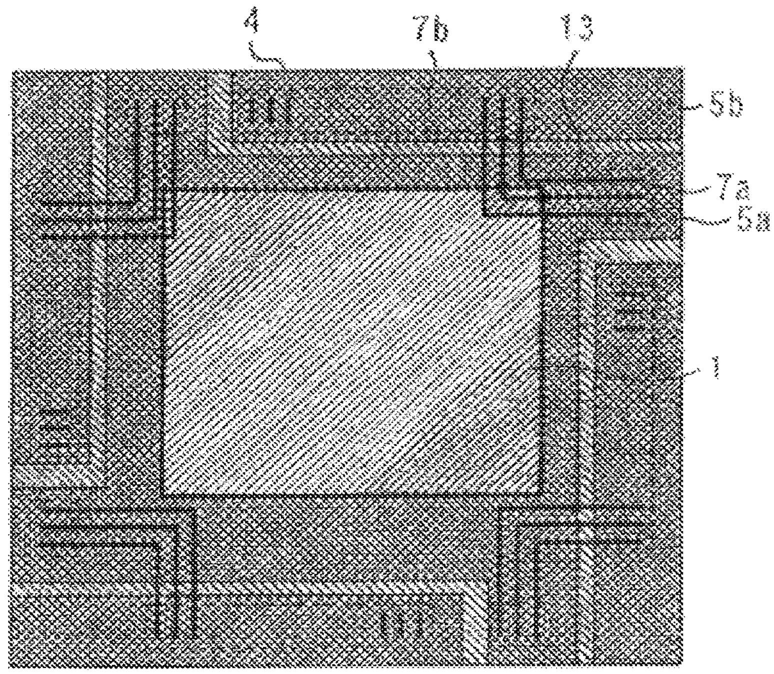


FIG. 13

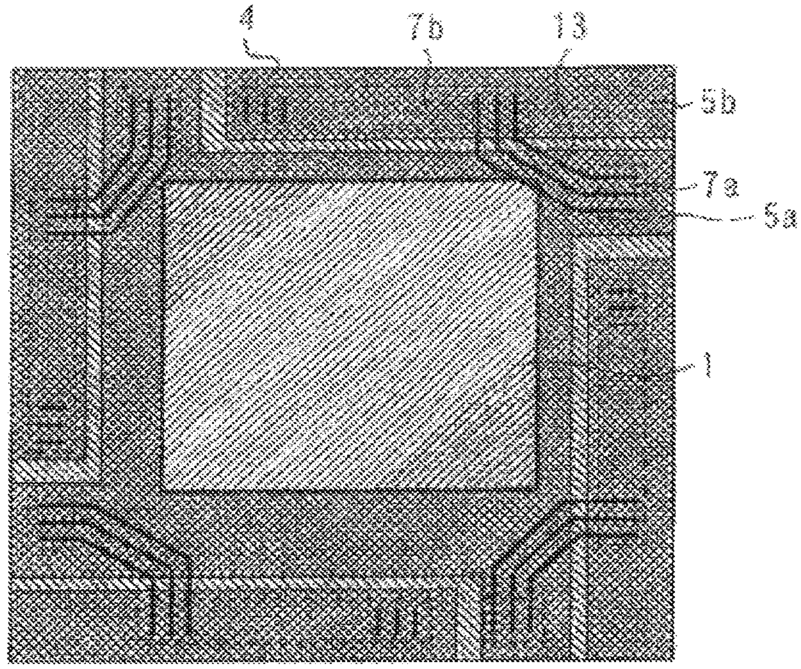
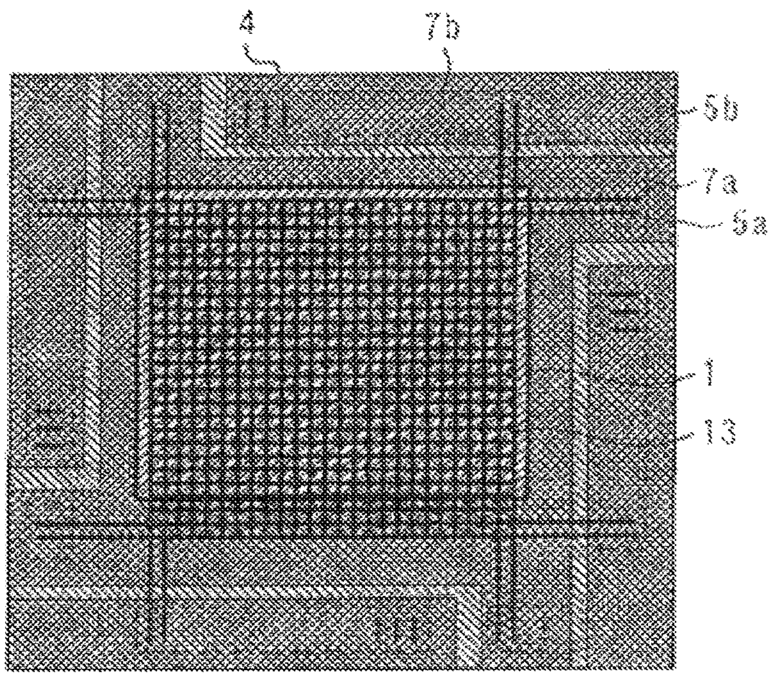


FIG. 14



SEMICONDUCTOR DEVICE

This divisional application claims the benefit of priority under 35 U.S.C. §120 from prior U.S. patent application Ser. No. 13/237,516, filed on Sep. 20, 2011. This application is also based upon and claims the benefit of priority under 35 U.S.C. §119 from prior Japanese Patent Application No. 2011-068214, filed on Mar. 25, 2011 in Japan. The entire contents of each of these applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device which can improve insulation resistance.

2. Background Art

A semiconductor device is available which includes a lower wiring covered with an inter-layer insulating film and an upper wiring placed thereon. On the surface of such a semiconductor device, a region other than a wire-bonded pad is covered with a semi-insulating protective film (e.g., see Japanese Patent Laid-Open No. 7-326744).

SUMMARY OF THE INVENTION

In the region where the upper wiring is etched, part of the inter-layer insulating film is also etched and thinned. Furthermore, the inter-layer insulating film is thinned in a stepped part of the lower wiring. Such a region with a thin inter-layer insulating film involves a problem that a leakage current flows via the semi-insulating protective film between the lower wiring and the upper wiring where a potential difference is produced, producing ESD (electrostatic discharge) destruction.

In view of the above-described problems, an object of the present invention is to provide a semiconductor device which can improve insulation resistance.

According to the present invention, a semiconductor device includes: a substrate; a lower wiring on the substrate; an inter-layer insulating film covering the lower wiring; first and second upper wirings on the inter-layer insulating film and separated from each other; and a semi-insulating protective film covering the first and second upper wirings, wherein the protective film is not provided in a region right above the lower wiring and between the first upper wiring and the second upper wiring.

The present invention makes it possible to improve insulation resistance.

Other and further objects, features and advantages of the invention will appear more fully from the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a top view illustrating a semiconductor device according to a first embodiment of the present invention.

FIG. **2** is an enlarged top view of the portion enclosed by a broken line in FIG. **1**.

FIG. **3** is a partially enlarged top view of FIG. **2**.

FIG. **4** is a cross-sectional view along A-A' of FIG. **3**.

FIG. **5** is a cross-sectional view illustrating a semiconductor device according to the comparative example.

FIG. **6** is a top view illustrating a modification example of the semiconductor device according to the first embodiment of the present invention.

FIG. **7** is a cross-sectional view along B-B' in FIG. **6**.

FIG. **8** is a top view illustrating a semiconductor device according to a second embodiment of the present invention.

FIG. **9** is a cross-sectional view along C-C' in FIG. **8**.

FIG. **10** is a top view illustrating a modification example of the semiconductor device according to the second embodiment of the present invention.

FIG. **11** is a top view illustrating a semiconductor device according to a third embodiment of the present invention.

FIG. **12** is a top view illustrating a modification example 1 of the semiconductor device according to the third embodiment of the present invention.

FIG. **13** is a top view illustrating a modification example 2 of the semiconductor device according to the third embodiment of the present invention.

FIG. **14** is a top view illustrating a modification example 3 of the semiconductor device according to the third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A semiconductor device according to the embodiments of the present invention will be described with reference to the drawings. The same components will be denoted by the same symbols, and the repeated description thereof may be omitted.

First Embodiment

FIG. **1** is a top view illustrating a semiconductor device according to a first embodiment of the present invention. A gate pad **1**, an emitter pad **2** and a sense pad **3** connected to a current temperature sensor (not shown), which are wire-bonded, are provided on a chip. The rest of the region other than these pads is covered with a protective film **4**.

The protective film **4** has a semi-insulating SInSiN film (refractive index: 2.2 to 2.7) having a film thickness of 2000 Å to 10000 Å and an insulating film (refractive index: 1.8 to 2.2) having a film thickness of 2000 Å to 10000 Å provided thereon to stabilize the withstand voltage and prevent polarization. A semi-insulating polysilicon (SIPOS: Semi-Insulating Polycrystalline Silicon) or the like may also be used instead of the SInSiN film.

FIG. **2** is an enlarged top view of the portion enclosed by a broken line in FIG. **1**. Aluminum wirings **5***a* and **5***b* separated from each other are connected at both ends of a gate resistor **7** via a contact electrode **6**. Part of the aluminum wiring **5***a* exposed from an opening of the protective film **4** constitutes the gate pad **1**. The aluminum wiring **5***b* is connected to a gate wiring **8**. The gate wiring **8** is connected to a trench gate **9** provided below the emitter pad **2**.

FIG. **3** is a partially enlarged top view of FIG. **2**. FIG. **4** is a cross-sectional view along A-A' of FIG. **3**. A gate oxide film **11** having a film thickness of 2000 Å to 10000 Å is provided on a Si substrate **10** and a gate resistor **7** made up of doped polysilicon having a film thickness of 500 Å to 5000 Å is provided thereon. The gate resistor **7** is covered with an inter-layer insulating film **12** made up of an oxide film having a film thickness of 2000 Å to 10000 Å. The inter-layer insulating film **12** is etched at both ends of the gate resistor **7** and the contact electrode **6** made of tungsten or the like is embedded. The inter-layer insulating film **12** is deposited through CVD (Chemical Vapor Deposition) and becomes thinner at the stepped part of the gate resistor **7**.

The aluminum wirings **5***a* and **5***b* having a film thickness of 1 μm to 10 μm, which are separated from each other, are provided on the inter-layer insulating film **12**. The aluminum wirings **5***a* and **5***b* are formed by forming an aluminum film through vapor deposition or sputtering and then etching the aluminum film. The aluminum wirings **5***a* and **5***b* are covered with the semi-insulating protective film **4**. However, the semi-insulating protective film **4** is not provided in a region right above the gate resistor **7** and between the aluminum wiring **5***a* and the aluminum wiring **5***b*.

Next, effects of the present embodiment will be described in comparison with a comparative example. FIG. **5** is a cross-sectional view illustrating a semiconductor device according to the comparative example. In the comparative example, the semi-insulating protective film **4** is provided in a region right above the gate resistor **7** and between the aluminum wiring **5***a* and the aluminum wiring **5***b*. However, when the aluminum wirings **5***a* and **5***b* are etched, part of the inter-layer insulating film **12** is also etched and thinned in this region. For this reason, in the comparative example, a leakage current flows via the semi-insulating protective film **4** between the gate resistor **7** and the aluminum wirings **5***a* and **5***b* where a potential difference is produced, producing ESD destruction.

On the other hand, the present embodiment does not provide the semi-insulating protective film **4** in the region right above the gate resistor **7** and between the aluminum wiring **5***a* and the aluminum wiring **5***b*. This makes it possible to extend the insulation distance between the gate resistor **7** and the aluminum wirings **5***a* and **5***b*, and thereby prevent ESD destruction. Thus, insulation resistance can be improved.

FIG. **6** is a top view illustrating a modification example of the semiconductor device according to the first embodiment of the present invention. FIG. **7** is a cross-sectional view along B-B' in FIG. **6**. The protective film **4** is not provided in the entire region right above the gate resistor **7**. This makes it possible to further improve insulation resistance.

Second Embodiment

FIG. **8** is a top view illustrating a semiconductor device according to a second embodiment of the present invention. FIG. **9** is a cross-sectional view along C-C' in FIG. **8**. Gate resistors **7***a* and **7***b* are provided on a Si substrate **10**. The gate resistors **7***a* and **7***b* are covered with an inter-layer insulating film **12**. Aluminum wirings **5***a* and **5***b* are provided on the inter-layer insulating film **12**. The aluminum wirings **5***a* and **5***b* are separated from each other and connected to the gate resistors **7***a* and **7***b* respectively via a contact electrode **6**. The aluminum wirings **5***a* and **5***b* are covered with a semi-insulating protective film **4**.

A trench wiring **13** is provided on the Si substrate **10** below a region between the aluminum wiring **5***a* and the aluminum wiring **5***b*. The trench wiring **13** connects the gate resistor **7***a* and the gate resistor **7***b*. The trench wiring **13** is formed by etching the Si substrate **10** by several μm to form a trench, oxidizing the side wall thereof to form an oxide film having a film thickness of 100 Å to 2000 Å and then embedding doped polysilicon.

The trench wiring **13** can extend the insulation distance between the gate resistors **7***a* and **7***b*, and the aluminum wirings **5***a* and **5***b*, and can thereby prevent ESD destruction. Therefore, insulation resistance can be improved.

FIG. **10** is a top view illustrating a modification example of the semiconductor device according to the second embodiment of the present invention. The trench wiring **13** is arranged in a mesh form. This reduces the resistance of the trench wiring **13**, and can thereby suppress the concentration of current.

Third Embodiment

FIG. **11** is a top view illustrating a semiconductor device according to a third embodiment of the present invention. An aluminum wiring **5***a* has a gate pad **1** exposed from a protective film **4**. A trench wiring **13** passes under the gate pad **1**. This makes it possible to reduce the area of elements. The rest of the configuration is the same as that of the second embodiment and can also obtain effects similar to those of the second embodiment.

FIG. **12** is a top view illustrating a modification example 1 of the semiconductor device according to the third embodiment of the present invention. The trench wiring **13** passes below a corner of the gate pad **1**. This avoids the trench wiring **13** from passing right below the gate pad **1**, and can thereby suppress influences of damage or the like. Furthermore, since the trench wiring **13** becomes shorter, the resistance of the trench wiring **13** can be reduced.

FIG. **13** is a top view illustrating a modification example 2 of the semiconductor device according to the third embodiment of the present invention. The trench wiring **13** is disposed diagonally with respect to the corner of the gate pad **1**. This further shortens the trench wiring **13**, and can thereby further reduce the resistance of the trench wiring **13**.

FIG. **14** is a top view illustrating a modification example 3 of the semiconductor device according to the third embodiment of the present invention. The trench wiring **13** is arranged in a mesh form below the gate pad **1**. Since the area of the gate pad **1** is large, many trench wirings **13** can be arranged. This causes the resistance of the trench wiring **13** to be reduced to a negligible level, and can thereby suppress the concentration of current.

In the semiconductor device according to the second and third embodiments, as in the case of the first embodiment, the semi-insulating protective film **4** may not be provided in a region right above the gate resistor **7** and between the aluminum wiring **5***a* and the aluminum wiring **5***b*. This can further improve insulation resistance.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is therefore to be understood that within the scope of the appended claims the invention may be practiced otherwise than as specifically described.

The entire disclosure of a Japanese Patent Application No. 2011-068214, filed on Mar. 25, 2011 including specification, claims, drawings and summary, on which the Convention priority of the present application is based, are incorporated herein by reference in its entirety.

What is claimed is:

1. A semiconductor device comprising:

a substrate;

first and second lower wirings on the substrate;

an inter-layer insulating film covering the first and second lower wirings;

first and second upper wirings on the inter-layer insulating film and separated from each other;

a trench wiring on the substrate below a region between the first upper wiring and the second upper wiring and connecting the first lower wiring and the second lower wiring; and

a semi-insulating protective film covering the first and second upper wirings.

2. The semiconductor device according to claim **1**, wherein the first upper wiring has a wire bonding area exposed from the protective film, and the trench wiring passes below the wire bonding area.

3. The semiconductor device according to claim **2**, wherein the trench wiring passes below a corner of the wire bonding area.

4. The semiconductor device according to claim **3**, wherein the trench wiring is disposed diagonally with respect to the corner of the wire bonding area.

5. The semiconductor device according to claim **1**, wherein the trench wiring is arranged in a mesh form.

* * * * *